AMENDMENTS TO THE SUBSTITUTE SPECIFICATION:

Please **replace** paragraph [0057] with the following amended paragraph:

E1

[0057] Next, as shown in FIG. 13, after ~~phosphor~~ phosphorus (P) ions are implanted into a part of the substrate 1 through the silicon oxide film 13, an n type scattering layer 3 is formed by annealing the substrate 1, where a dose quantity of ~~phosphor~~ phosphorus ion is 4.5 x 1012 cm^{-2}, and implantation energy thereof is 360 keV.

Please **replace** paragraph [0058] with the following amended paragraph:

E2

[0058] Then, ~~phosphor~~ phosphorus (P) ions are implanted into a part of the substrate 1, and boron (B) ions are implanted into another part. Thereafter, an n type well 4 and a p type well 5 are formed by annealing the substrate 1. At this time, a dose quantity of ~~phosphor~~ phosphorus ion is 1.2 x 13^{13} cm^{-2} and implantation energy thereof is 360 KeV while a dose quantity of boron ion are 0.8 x 10^{13} cm^2 and implantation energy thereof is 200 keV.

Please **replace** paragraph [0062] with the following amended paragraph:

E3

[0062] Next, n type poly-crystalline silicon film (not shown) of about 200 nm in film thickness formed by doping ~~phosphor~~ phosphorus (P) is deposited on the substrate 1 by using the CVD method, and then, a silicon oxide film 14 of about 100 nm in film thickness is deposited at an upper part of this poly-crystalline

silicon film by using the CVD method. Thereafter, a photo-resist film is masked, and respective parts of the silicon oxide film 14, the poly-crystalline silicon film and gate insulation film 7 are etched, and thereby the gate electrode 10 and the gate insulation film 7 are formed, respectively. To this gate electrode 10, a rewriting high voltage (Vpp) or power supply voltage (Vcc) is supplied through the constant voltage generation circuit shown in FIG. 2 at the time of data rewriting (writing and erasing). And, electrons or positive holes are implanted into the gate insulation film 7 at a lower part of the gate electrode due to a tunnel effect.

E3

Please **replace** paragraph [0066] with the following amended paragraph:

[0066] Next, as shown in FIG. 16, boron (B) ions are implanted into the n type scattering layer 3 and the n type well 4 to form a p^- type semiconductor region 16 with low impurity concentration. ~~Phospher~~ Phosphorus (P) ions are implanted into the p type well 5 to form the n^- type semiconductor region 17 with low impurity concentration.

E4

Please **replace** paragraph [0067] with the following amended paragraph:

[0067] Next, as shown in FIG. 17, each of side wall spacers 18 is formed on respective side walls of gate electrodes 10 and 11. Then, boron (B) ions are implanted into the n type scattering layer 3 and the n type well 4 and thereby a p^- type semiconductor region (source and drain) 19 with high impurity concentration is, respectively, formed in a memory cell forming region and a peripheral circuit forming region. Although not shown in the figure, a p^+ type semiconductor region

E5

19 is also formed at a part of the p type well 5 in the zener diode forming region (at the lower part of the connection hole 25 shown in FIG. 4) at this time. In addition, arsenic (As) ions and ~~phosphor~~ phosphorus (P) ions are implanted into the p type well 5, and thereby a n^+ type semiconductor region (source and drain) 20 with high impurity concentration is formed in a peripheral circuit forming region. And, the n^+ type semiconductor region 20 with high impurity concentration is formed in a zener diode forming region. The side wall spacers 18 are formed by performing isotropic etching of a silicon oxide film (not shown) deposited on the substrate 1 by using the CVD method. At this time, dose quantity of boron ion is defined as 2×10^{15} cm^{-2} and implantation energy thereof is defined as 10 keV. Dose quantity of arsenic ion is defined as 3×10^{15} cm^{-2} and implantation energy thereof is defined as 60 keV. And, dose quantity of ~~phosphor~~ phosphorus ion is defined as 5×10^{13} cm^{-2} and implantation energy thereof is defined as 60 keV.

AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Claims 1-3 - (Canceled)

4. (Withdrawn) A semiconductor integrated circuit device according to claim 1, wherein each of said plurality of first connection holes is spaced from each other so that a pitch between the adjacent first connection holes is greater than a minimum pitch between connection holes of the circuit.

EB

5. (Withdrawn) A semiconductor integrated circuit device according to claim 4, wherein the pitch between said adjacent first connection holes is two times and more of the minimum pitch between the connection holes of said circuit.

6. (Withdrawn) A semiconductor integrated circuit device according to claim 5, wherein the pitch between said adjacent first connection holes is three times and more of the minimum pitch between the connection holes of said circuit.

7. (Withdrawn) A semiconductor integrated circuit device according to claim 6, wherein the pitch between said adjacent first connection holes is four times and more of the minimum pitch between the connection holes of said circuit.

8. (Withdrawn) A semiconductor integrated circuit device comprising: a semiconductor substrate of a first conductivity type; a zener diode comprised of a first semiconductor region of a second conductivity type formed in a primary face of said semiconductor substrate, and a second semiconductor region of said first conductivity type formed in said semiconductor substrate at a bottom portion of said first semiconductor region and being smaller than said first semiconductor region in an area surrounding a planar pattern thereof,

E6

wherein a plurality of first connection holes for electrically connecting said first semiconductor region and a wire to each other are arranged in a region being outside a junction formed between said first semiconductor region and said second semiconductor region, and wherein each of said plurality of first connection holes is spaced apart from others of said connection holes so that a pitch between the adjacent first connection holes is greater than a maximum pitch between connection holes of the circuit.

9. (Withdrawn) A semiconductor integrated circuit device according to claim 8, wherein a junction depth of said first semiconductor region in a region in which said first and second semiconductor regions form a junction is shallower than that of said semiconductor region in a region in which said semiconductor substrate and said first semiconductor region form a junction.

10. (Withdrawn) A semiconductor integrated circuit device according to claim 8, wherein each of said plurality of first connection holes is equal to and smaller than a connection hole arranged with a minimum pitch of the circuit in diameter.

11. (Withdrawn) A semiconductor integrated circuit device comprising:

a plurality of first connection holes for electrically connecting a first wire and a first semiconductor region formed in a first region of a primary face of a semiconductor substrate, to each other therethrough; and

a plurality of second connection holes for electrically connection a second wire and a second semiconductor region formed in a second region of the primary face of the semiconductor substrate, to each other therethrough, wherein each of said plurality of first connection holes is spaced from others of said first connection holes so that a pitch between the adjacent first connection holes is greater than a minimum pitch between connection holes of the circuit, and wherein each of said plurality of second connection holes is spaced from others of said second connection holes so that a pitch between adjacent second connection holes substantially equal to the minimum pitch of the connection holes of the circuit.

E6

Claims 12-14 (Canceled)

15. (Withdrawn) A semiconductor integrated circuit device comprising:

a first semiconductor region of a first conductivity type formed in a primary face of a semiconductor substrate;

a second semiconductor region of said first conductivity type formed on said semiconductor substrate at an upper part of said first semiconductor region, said second semiconductor region having a higher impurity concentration than said first semiconductor region;

a third semiconductor region of a second conductivity type formed in said

semiconductor substrate at upper parts of said first and second semiconductor regions;

a first insulation film formed on said primary face of said semiconductor substrate;

a first connection hole comprised of a plurality of connection holes formed in said first insulation film at said upper part of said first semiconductor region; and

a second connection hole comprised of a plurality of connection holes formed in said first insulation film at said upper part of said third semiconductor region, wherein said second connection hole is formed in an upper part of a region in which said first semiconductor region and said third semiconductor region from a junction.

16. (Withdrawn) A semiconductor integrated circuit device according to claim 15, wherein a first electrically conductive connection body of said first conductivity type and a second electrically conductive connection body of said second conductivity type are provided inside said first and second connection holes, respectively, and wherein a first wire electrically connected to said first semiconductor region via said first electrically conductive connection body, and a second wire electrically connected to said third semiconductor region via said second electrically connecting connection body are formed at said upper part of said first insulation film.

17. (Withdrawn) A semiconductor integrated circuit device according to claim 16, wherein said first semiconductor region is comprised of a fourth

semiconductor region of said first conductivity type, and a fifth semiconductor region electrically connected to said first electrically conductive connecting body via said fourth semiconductor region, wherein an impurity concentration of said fifth semiconductor region is lower than an impurity concentration of said fourth semiconductor region.

18. (Withdrawn) A semiconductor integrated circuit device according to claim 15, wherein said first and second connection holes are formed by using a photo-resist film as a mask and by dry etching said first insulation film.

19. (Withdrawn) A semiconductor integrated circuit device comprising:

a first semiconductor region formed in the primary face of a semiconductor substrate;

a second semiconductor region of a first conductivity type formed on said semiconductor substrate at an upper part of said first semiconductor region;

a third semiconductor region of a second conductivity type formed on said semiconductor substrate at upper parts of said first and second semiconductor regions;

a first insulation film formed on said primary face of said semiconductor substrate;

a first connection hole comprised of a plurality of connection holes formed on said first insulation film at said upper part of said first semiconductor substrate; and

a second connection hole comprised of a plurality of connection holes formed on said first insulation film at an upper part of said third semiconductor

region, wherein a minimum pitch between adjacent connection holes of said second connection hole is greater than a minimum pitch between adjacent connection holes of said first connection hole.

20. (Withdrawn) A semiconductor integrated circuit device according to claim 19, wherein said first semiconductor region is a semiconductor region of said second conductivity type and is lower than said second semiconductor region in a impurity concentration.

E6

21. (Withdrawn) A semiconductor integrated circuit device according to claim 19, wherein said first semiconductor region is a semiconductor region of said second conductivity type that forms a collector region of a bipolar transistor, said second semiconductor region is a semiconductor region of said first conductivity type that forms a base region of said bipolar transistor, and said third semiconductor region is a semiconductor region of said second conductivity type that forms an emitter region of said bipolar transistor.

Claim 22. (Canceled)

23. (Withdrawn) A semiconductor integrated circuit device according to claim 22, wherein each of said plurality of first connection holes is spaced from others so that a pitch between adjacent first connection holes is greater than a minimum pitch between connection holes of the circuit.

Claims 24-38 (Canceled)

39. (New) A semiconductor integrated circuit device comprising:

a semiconductor substrate of a second conductivity type;

at least a first zener diode and a second zener diode connected in series and comprised of

(i) a first well region of a first conductivity type formed in said semiconductor substrate,

(ii) at least two spaced-apart, second well regions of said second conductivity type formed in said first well region, each of said second well regions being associated with different ones of said zener diodes,

E6

(iii) first semiconductor regions of said first conductivity type formed in said second well regions, respectively, and

(iv) second semiconductor regions of said second conductivity type formed at a bottom portion of said first semiconductor regions, respectively, and each being smaller in area, defined by a planar pattern thereof, than said first semiconductor region corresponding thereto;

an insulation film formed over a primary face of said semiconductor substrate;

a plurality of first connection holes for providing electrical connections therethrough to said first semiconductor regions and a plurality of second connection holes for providing electrical connections therethrough to said second well regions being formed in said insulation film; and

a wiring formed over said insulation film and connecting said first connection holes which are for electrical connection to the first semiconductor region of said first zener diode and said second connection holes which are for electrical connection to the second well region of said second zener diode,

wherein said first connection holes associated with said first zener diode are arranged in a region located outside a junction formed between said first semiconductor region and said second semiconductor region of said first zener diode,

wherein a first PN junction is formed between ones of said first semiconductor regions and corresponding ones of said second semiconductor regions and functions as a diode device, and a second PN junction is formed between said first well region and said second well regions, respectively, and has a breakdown voltage greater than that of said first PN junction, and

wherein a junction depth of each of said first semiconductor regions in a region in which said first PN junction is formed is shallower than that of each of said first semiconductor regions in a region in which said first PN junction is not formed.

40. (New) A semiconductor integrated circuit device according to claim 39, wherein said second semiconductor regions are arranged substantially at a center location of said first semiconductor regions, respectively, and said plurality of first connection holes are arranged at a periphery of said first semiconductor regions, respectively.

41. (New) A semiconductor integrated circuit device according to claim 40, wherein said second semiconductor regions have an impurity concentration higher than that of said second well regions.

42. (New) A semiconductor integrated circuit device according to claim 39, wherein said second semiconductor regions have an impurity concentration higher than that of said second well regions.

43. (New) A semiconductor integrated circuit device according to claim 39, wherein said first conductivity type is taken from one of an n-type and a p-type conductivities, and said second conductivity type is the other of said n-type and p-type conductivities.

44. (New) A semiconductor integrated circuit device comprising:

a semiconductor substrate of a second conductivity type;

a first impurity region of a first conductivity type formed in said semiconductor substrate,

a plurality of diodes connected in series, at least a first diode and a second diode of said plurality of diodes include, respectively,

(i) a second impurity region of a second conductivity type formed in said first impurity region,

(ii) a third impurity region of a first conductivity type formed in said second impurity region, and

(iii) a fourth impurity region of a second conductivity type formed in said second impurity region under said third impurity region,

wherein said first impurity region is common to said at least first and second series-connected diodes;

an insulation film formed over a primary face of said semiconductor substrate;

first plugs for electrically connecting therethrough to said third impurity region and second plugs for electrically connecting therethrough to said second impurity region of said first and second diodes, respectively, said first and second plugs being formed in said insulation film; and

a conductive layer formed over said insulation film and connected via ones of said first plugs to said third impurity region of said first diode and connected via ones of said second plugs to said second impurity region of said second diode,

wherein said third impurity region has a first portion and a second portion, said first portion is that in which a first PN junction is formed between said third and fourth impurity region and said second portion is that below which said fourth impurity region is not formed,

wherein a junction depth of said first portion is shallower than that of said second portion, and

wherein said second portion is formed outside said first portion, and said first plugs are formed over said second portion of said third impurity region.

45. (New) A semiconductor integrated circuit device according to claim 44, wherein at least said first and second diodes are zener diodes, respectively.

46. (New) A semiconductor integrated circuit device according to claim 44, wherein said second portion is formed in a periphery of said first portion so as to surround said first portion, and said first plugs are arranged over said

second portion so as to surround said first portion.

47. (New) A semiconductor integrated circuit device according to claim 46, wherein said fourth impurity region has an impurity concentration higher than that of said second impurity region.

48. (New) A semiconductor integrated circuit device according to claim 47, wherein said first conductivity type is taken from one of an n-type and a p-type conductivities, and said second conductivity type is the other of said n-type and p-type conductivities.

49. (New A semiconductor integrated circuit device according to claim 46, wherein a breakdown voltage of a second PN junction formed between said first and second impurity regions is greater than that of said first PN junction.

50. (New) A semiconductor integrated circuit device according to claim 44, wherein said fourth impurity region has an impurity concentration higher than that of said second impurity region.

51. (New) A semiconductor integrated circuit device according to claim 50, wherein a breakdown voltage of a second PN junction formed between said first and second impurity regions is greater than that of said first PN junction.

52. (New) A semiconductor integrated circuit device according to claim 44, wherein a breakdown voltage of a second PN junction formed between said

first and second impurity regions is greater than that of said first PN junction.

53. (New) A semiconductor integrated circuit device comprising:

a first diode and a second diode connected in series and commonly formed in a first well region of a first conductivity type, said first well region being formed on a semiconductor substrate, and said first diode and said second diode, respectively, comprising

(i) a second well region of a second conductivity type formed in said first well region,

(ii) a first semiconductor region of a first conductivity type formed in said second well region, and

(iii) a second semiconductor region of a second conductivity type, said second semiconductor region being formed in said second well region and under said first semiconductor region;

an insulation film formed over a primary face of said semiconductor substrate;

a plurality of first connection holes for providing electrical connections therethrough to said first semiconductor region and a plurality of second connection holes for providing electrical connections therethrough to said second well region being formed in said insulation film; and

a wiring formed on said insulation film and connecting said first connection holes which are for electrical connection to said first semiconductor region of said first diode and said second connection holes which are for electrical connection to said second well region of said second diode,

wherein said second semiconductor region has an impurity concentration

higher than that of said second well region,

wherein said first semiconductor region has a first portion and a second portion, said first portion is that below which said second semiconductor region is formed and said second portion is that below which said second semiconductor region is not formed,

wherein a first PN junction is formed between said second semiconductor region and said first semiconductor region at said first portion and constitutes a zener diode,

wherein a junction depth of said first portion is shallower than that of said second portion, said second portion is formed in a periphery of said first portion so as to surround said first portion,

E6

wherein said plurality of first connection holes are arranged over said second portion so as to surround said first portion, and

wherein a second PN junction is formed between said first well region and said second well region and has a breakdown voltage greater than that of said first PN junction.

54. (New) A semiconductor integrated circuit device according to claim 53, wherein said first and second conductivity types are a p-type conductivity and an n-type conductivity, respectively.

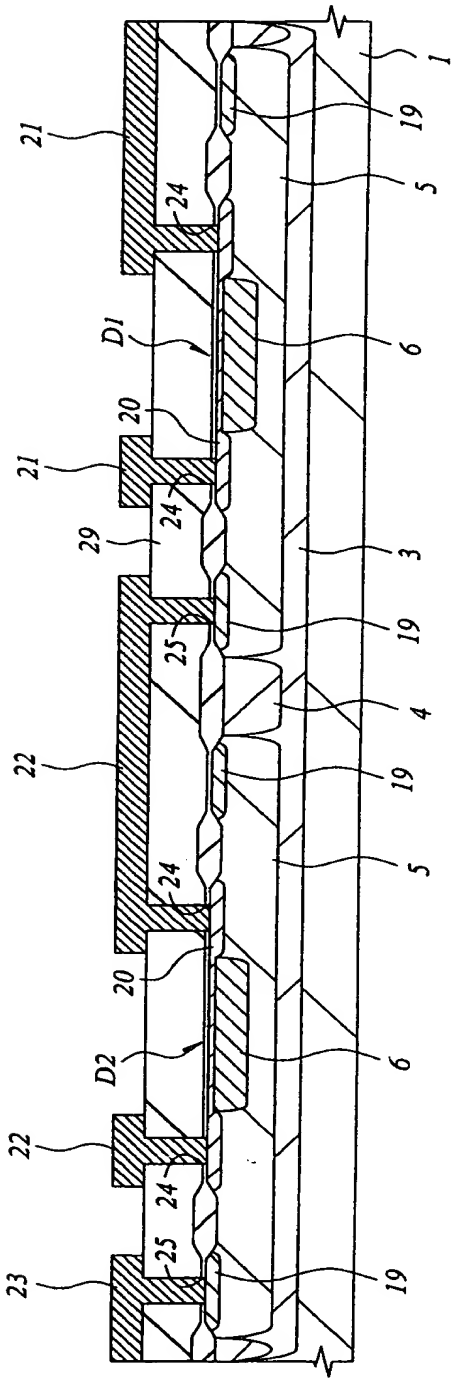
55. (New) A semiconductor integrated circuit device according to claim 53, wherein said first and second conductivity types are a n-type conductivity and an p-type conductivity, respectively.

AMENDMENTS TO THE DRAWINGS:

The attached sheet of drawings includes the earlier approved changes to Fig. 4. This sheet, which includes Fig. 4, replaces the originally submitted drawing sheet of that Figure. In Fig. 4 a labeling correction of the third contact hole from the left in that Figure was effected.

Attachment: **Replacement Sheet**

FIG.4



REMARKS

Formal acceptance of the above amendments as a submission in connection with USPTO RCE practice is respectfully requested.

In the Specification, the named paragraphs have been amended to correct minor informalities. Acceptance of these revisions is respectfully requested.

The accompanying replacement sheet of drawings directed to Fig. 4 thereof formally includes the earlier revision proposed in the paper submitted on January 21, 2003, which was approved for entry in form PTO-326 in connection with the Final Office Action dated April 8, 2003. Acceptance and formal entry therefor of the same is respectfully requested.

The status of the claims are given hereinabove. Namely, claims 1-3, 22, 24, 26, 27 and 29-38 are being canceled and claims 39-55 are being newly presented as a substitute therefor. (Claims 12-14, which were previously withdrawn, as a result of a restriction requirement, were earlier canceled. Claims 4-11, 15-21 and 23 remain withdrawn as a result of an earlier supplementing election/restriction requirement.)

As indicated above, the previously rejected claims 1-3, 22, 24, 26, 27 and 29-38 were canceled in favor of newly presented substitute claims 39-55. Accordingly, all the previously standing rejections under items 4-6, covering pages 3-7 of the Final Office Action have been rendered moot. Likewise, the outstanding objection noted, under item 2, on pages 2-3 of the Final Office Action was also rendered moot in view of the present canceling of the claims in

question. The canceling of the claims in favor of the newly presented substitute claims should not be construed as an acquiescence as to the merits of the previously standing objection/rejections to those claims. Rather, applicants as a result of a further careful review of the original disclosure, have drafted a new, substitute set of claims in consideration of more clearly defining the invention intended to be covered by those claims which are presently canceled. Accordingly, examination as well as favorable action therefor on the newly presented claims 39-55 is respectfully requested.

It is submitted, the invention according to claims 39-55 is defining over the art documents including as that applied in the previously standing Final Office Action. The following supportive discussion directed thereto is being provided.

Each of the newly presented independent claim groups 39+, 44+ and 53+ is intended to cover a semiconductor IC device scheme calling for two or more series-connected diodes such as zener diodes which are formed within a same well region, an example of a construction of which is given with regard to Figs. 3 and 4 of the drawings, although not limited thereto, which show a construction of series-connected diodes such as the two-stage zener diode for the clamping circuit shown in Fig. 2 of the drawings. As can be seen from Fig. 4 of the drawings, both the diode D1 and the diode D2 construction are implemented within the same well 3, in Fig. 4. Insofar as it relates to the present claims, diodes D2 and D1 correspond to the first diode (first zener diode) and second diode (second zener diode) of the claims when considering their series connection via the wiring (conductive layer) such as the interconnecting wire 22 shown in Fig. 4 of the drawings, which connects n^+ region 20 of diode D2 to the

p well 5 associated with diode D1 via the respective contact hole electrical connections.

The device according to independent claim 39 calls for "at least a first zener diode and a second zener diode connected in series" and moreover, calls for this series-connection to be comprised of

(i) a first well region of a first conductivity type formed in the semiconductor substrate (which is of a second conductivity type),

(ii) at least two spaced-apart, second well regions of the second conductivity type formed in the first well region, each of the second well regions being associated with different ones of the series-connected zener diodes,

(iii) first semiconductor regions of the first conductivity type formed in the second well regions, respectively, and

(iv) second semiconductor regions of the second conductivity type formed at a bottom portion of the first semiconductor regions, respectively, and each being smaller in area defined by a planar pattern thereof, then the first semiconductor region corresponding thereto.

Such a series-connection scheme including at least a first and a second zener diode can be seen with regard to Figs. 3 and 4 of the drawings, although not limited thereto, in which the semiconductor substrate of a second conductivity type relates to the p substrate 1, the "first well region" relates to the n-type scattering 3 layer which is doped with phosphorous ions, the second well region associated with each of the series-connected zener diodes can be seen with regard to the two p wells 5, both of which are formed within the n-type scattering layer 3; the first semiconductor regions can be seen with regard to n^+ regions 20 and the p^+ region 6 which are formed beneath regions 20 relate to the "second semiconductor regions," according to independent claim 39.

The device scheme called for in claim 39 also features an insulation film such as silicon oxide 29, a plurality of first connection holes (e.g., 24) for

providing electrical connections therethrough to the first semiconductor regions (e.g., 20) and a plurality of second connection holes (e.g., 25) for providing electrical connections therethrough to the "second well regions" (e.g., p wells 5). Also, claim 39 calls for a wiring (e.g., 22) formed over the insulating film (e.g., 29) and connecting the first connection holes (e.g., 24) which are for electrical connection to the first semiconductor region of the first zener diode (e.g., D2) and the "second connection holes" (e.g., 25) which are for electrical connection to the second well region (e.g., 5) of the second zener diode (D1) in Figs. 2, 3 and 4.

Further, the invention according to claim 39 requires a structural configuration in which the "first connection holes" associated with the first zener diode are arranged outside the PN junction formed between the first and second semiconductor regions of that zener diode and that a junction depth of each of the first semiconductor regions at a location thereof where it forms a junction with the second semiconductor region is shallower than that of each such first semiconductor region in the region in which such junction is not formed. This can be seen from Fig. 4 of the drawings which shows a relatively shallower thickness of n^+ region 20 at a location thereof where the p^+ region 6 is formed than that at an outer periphery thereof, where such junction is not formed. Also according to claim 39, the invention calls for a breakdown voltage at a PN junction formed between the first and second well regions to be greater than that formed across the PN junction formed between the first and second semiconductor regions.

According to claim 40 (dependent on claim 39), the invention further limits the "second semiconductor regions" (e.g., regions 6) to be arranged substantially

at a center location of the "first semiconductor regions" (e.g., 20) and for the plurality of "first connection holes" (e.g., 24) to be arranged at a periphery with regard to each of the "first semiconductor regions" (e.g., 20). Consistent with the Specification and Fig. 4 of the drawings, the "second semiconductor regions" have an impurity concentration higher than that of the "second well regions" (e.g., p wells 5) and the "second semiconductor regions" (e.g., p^+ regions 6) have an impurity concentration higher than that of the "second well regions" (e.g., p wells 5) (see claims 41 and 42).

Supportive discussion regarding the above-noted featured aspects are provided, for example, in paragraphs [0046] - [0048] of the Substitute Specification as it relates to the embodiment shown in Figs. 2, 3 and 4 of the drawings. Namely, paragraphs [0045] and [0046] give a detailed discussion of the example device structure such as it relates to Figs. 3 and 4 of the drawings. The conductivity type relationships of the particular regions/well regions as well as the size/placement relationships between that of the p^+ region 6 and that of n^+ region 20 is given in paragraph [0045] and a depth relationship associated with different parts of region 20 is given in paragraph [0046]. The wire connections of the invention, such as shown in Figs. 3 and 4 of the drawings, are discussed in paragraphs [0047] / [0048], etc. Such featured aspects, although in a somewhat modified form thereof, along with additional featured aspects of the originally disclosed invention are also covered in claims 44-52 as well as with regard to claims 53-55.

With regard to claims 44+, the semiconductor construction recited is in connection with each of the individual ones of a first diode and a second diode which are in series-connection. According to claims 44+, rather than calling for

first and second well regions, the structure calls for first and second impurity regions, respectively. Namely, with regard to claims 44+, each one of the first and second diodes in the series-connection of diodes is structurally configured to include a second impurity region of a second conductivity type formed in a first impurity region of a first conductivity type and, also, calls for a third impurity region of a first conductivity type formed in the second impurity region and a fourth impurity region of a second conductivity type formed in the second impurity region under the third impurity region, the "first impurity region" being common to at least the first and second series-connected diodes. Regions 3, 5, 20 and 6, according to the example showing in Fig. 4 of the drawings, relate to the first through fourth impurity regions according to claims 44+, respectively. Also according to claim 44+, the invention calls for "first plugs for electrically connecting therethrough to the third impurity region and second plugs for electrically connecting therethrough to the second impurity region of the first (e.g., D2) and second (e.g., D1) diodes, respectively, the plural first and second plugs being formed in the insulating film. Rather than calling for a wiring, the invention according to claim 44 calls for a "conductive layer" for effecting a similar connection via the plugs as that shown with regard to Figs. 3 and 4 of the drawings, although not limited thereto.

The invention according to claims 53+ calls for a series-connection of a first diode and a second diode which are commonly formed in a first well region, each of the first and second diodes being constructed in the manner consistent with that shown in Fig. 4 of the drawings, although not limited thereto. With regard to claims 53+, the conductivity type convention employed therein is consistent with that according to base claim 39, although in a complementary

fashion thereto. It is submitted, the invention as now called for in claims 39+, 44+ and 53+ is clearly defining over the art documents as previously cited.

When constructing diodes such as zener diodes to be included in a series-connection scheme as that shown with regard to Fig. 4 of the drawings, although not limited thereto, it is necessary for the doping concentrations of the different impurity regions to be such that the breakdown voltage effected between the n region 3 and p well 5 is greater than that effected across the junction between p^+ region 6 and n^+ region 20. Such is achieved in connection with the invention called for in claims 39+, 44+ and 53+. When considering the series-connection of plural such diodes, also, the breakdown voltage requirements become such as that shown in Fig. 1 exhibit attached to the amendment filed on December 23, 2002. That sketch 1, for example, relates to the series-connection of two zener diodes such as shown in Figs. 2 and 4 of the drawings, in which diodes D1 and D2 relate to the zener PN junctions formed between that of the P^+ region 6 and n^+ region 20 with regard to the D1 and D2 portions of Fig. 1, respectively, while D1' relates to a junction effected between n region 3 and p well 5 in the D1 portion, and D2' relates to a junction formed between the n region 3 and the p well 5 with regard to the portion D2. The breakdown voltage of D1' must be greater than or equal to the breakdown voltage of the corresponding zener diode junction associated with D1. Further, the breakdown voltage of D2' should also be at least as large as the overall breakdown voltage of D1 + D2. Accordingly, it is noted that the p wells 5, according to the example showings with regard to Figs. 3-4, have a lower doping concentration than that of the p^+ region 6 which leads to a series-connection of zener diodes that operates satisfactorily. It is submitted, such a scheme as that

now called for in claims 39+, 44+ and 53+ could not have been achievable in the manner as that alleged in the previously standing Final Office rejections. This is addressed in connection with the discussion which follows, directed to the art documents cited in the previously standing Final Office rejections.

Sugawara et al (JP 63-66974)

According to the embodiment disclosed in Sugawara et al, not only is the construction of the zener diode therein unlike that presently called for in each of the claims but, moreover, Sugawara et al also failed to teach a scheme featuring two or more diodes such as two or more zener diodes in series-connection and which are mutually formed within the same well region, the well region being formed in a semiconductor substrate, such as that called for with regard to newly presented claims 39+, 44+ and 53+. According to the sectional view in Fig. 2 of Sugawara et al, it is observed that n^+ impurity region 10 covers a wider area than that covered by p^- region 9 which underlies n^+ region 10. It is noted that the depletion layer 11, which extends deeper into the substrate, surrounds p^- region 9. Also according to Figs. 1 and 2 of Sugawara et al, the connection holes 6 are formed within the area covered by the deeper region 9. Clearly, therefore, the present invention is defining thereover.

Howard et al (US 3,881,179)

The embodiment shown in Fig. 1 of Howard et al shows a zener diode structure having an n-type cathode 32, a p-type conductive portion 21 and a p^+ type anode 22 connected with the p type conductive portion 21. As can be seen from the Fig. 1 illustration thereof, the n type cathode region 32 has an outer periphery surrounding that of the p type impurity region 22. Also, the connection hole C for the cathode is formed on that deeper peripheral region. However,

Howard et al, like that of Sugawara et al, failed to teach designing a structure including at least two diodes in series such as two series connected zener diodes which are also formed within a same well region of a semiconductor substrate. There is neither specific discussion nor suggestion in Howard et al of designing a scheme as that presently called for in claims 39+, 44+ and 53+. If one, *arguendo*, were to attempt to employ Howard et al's zener diode as part of a series connection of zener diodes in the manner as that presently called for, it would be quite difficult for Howard et al's zener diode to keep the stability in the breakdown voltage between the n^+ buried layer 12 and the p^+ anode 22 due to the presence of the high concentration associated with the p^+ anode 22. Clearly, therefore, one of ordinary skill would not have been led to the present invention based on Howard et al's teachings.

Takahashi (US 6,114,872)

Takahashi was cited as disclosing the use of zener diodes in the clamping circuit such as for a differential input circuit. (Fig. 13 and column 9, line 66, to column 10, line 4, in Takahashi.) Takahashi, however, neither disclosed nor suggested a series-connection of zener diodes constructed within the same well region which is contained within a semiconductor substrate, as that presently called for and which construction further calls for, for example, an n-type impurity region having a portion which is extended deeper into the well region and surrounds an underlying p type impurity region such as that presently called for and as shown by the example embodiment in Fig. 4 of the drawings, although not limited thereto. It is submitted, therefore, Takahashi also failed to disclose or suggest such a scheme as that now called for in claims 39+, 44+ and 53+.

Villa et al (US 5,756,387)

Villa et al was cited in connection with its teachings of a zener diode structure such as shown in Fig. 5 thereof. According to this showing, Villa et al's structure features a region having a shallow n^+ type impurity region surrounded by a deeper n type impurity region, both of which form a junction with the same p region, contrary to that presently called for. Villa et al neither disclosed nor suggested a scheme also calling for series-connected diodes such as zener diodes to be formed in the same well region (or common impurity region) in a semiconductor substrate as that presently called for in claims 39+, 44+ and 53+. In that regard, it is noted that the zener diode construction taught by Villa et al features separate/isolated regions, the regions being completely isolated by p^+ plugs, as can be seen from Fig. 5 in Villa et al. In view of this, it is clearly apparent that Villa et al gave no consideration to the construction of series-connection of zener diodes.

As was shown hereinabove, none of the above-noted art documents, which were cited in the previously standing Final Office Action rejections, disclosed or suggested a semiconductor IC device scheme calling for the construction of a series-connection of at least two diodes such as zener diodes in a manner as that presently called for in claims 39+, 44+ and 53+, and as discussed above. In view of at least the above-noted deficiencies even if one of ordinary skill would have attempted to employ the teachings of different ones of the above-cited references to modify the construction of a zener diode, there still would not have been effected nor realizable therefrom a series construction of two or more such diodes or zener diodes as that presently called for in the newly presented claims. Accordingly, examination as well as a favorable action

therefor on the newly presented claims 39-55 and an early formal Notification of Allowability of the above-identified application is respectfully requested. Examination as well as favorable action therefor is also respectfully requested with regard to the presently withdrawn claims.

To the extent necessary, applicants petition for an extension of time under 37 CFR §1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees to the Deposit Account of Antonelli, Terry, Stout & Kraus, LLP, Dep. Acct. No. 01-2135 (843.39542X00), and please credit any excess fees to such deposit account.

Respectfully submitted,
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